Fast TR pulse Task Description

**Objective:** Design, build and test a circuit that level shifts the 0/3v logic state out of the FPGA VHDC port to 0/5v states where good 20 nS pulse fidelity is maintained. The fast RF switch needs atleast 3.5v to guarantee switching.

**Purpose:** Gates the Transmit-Receive (TR) pulse which is only 20 nS wide to the ultrafast RF SP2T TR switch. Pulse shape fidelity needs to be maintained.

**Approach:** Design circuit in LTSpice that uses a MOSFET to switch in a 5v logic level. MOSFET is switched by the 0/3v FPGA signal. A circuit design was done last year by Olivier B. , so he should have a copy somewhere you can use as a reference. The MOSFET selected was very small and was not able to be soldered successfully. Suggest procuring MOSFET already on the board as a starting component. Signal line impedance between the FPGA input and at output at TR switch need be considered to maintain good fidelity. In past a pulse generator was used to generate this signal as contingency, however if we get started early we should be able to get a circuit to work so pulse gen is not required.